CMP and Wafer Grinding
Applications and Challenges in 3D Interconnect: An Overview

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Outline

• SEMATECH background
• 3D integration benefits and goals
• Via-mid TSV process overview
• Bonding and Grind
  • Permanent Bonding
  • Temporary Bonding
  • Grinding issues
• CMP steps
  • TSV polish
  • M1 polish
  • TSV reveal polish
  • Backside planarization
  • Backside metal polish
• Conclusions

• SEM image shows 5x50 micron through-Si vias (TSVs) built at SEMATECH
SEMATECH – 3D Interconnect Program

3D TSV program
• Materials development
• Equipment development
• Unit process development
• Integration
• Test vehicles
• Reliability
• Ecosystem development

Collaboration with
• Member companies
• Suppliers (equipment, materials, processes)
• Universities
• Industry organizations (associations, standards bodies, consortia)
3D Integration

- Wire bond 3D

- TSV 3D

- 3D integrated circuit with TSV
- Memory on logic TSV stack

- 3D integration benefits
  - Increased density
  - Shorter interconnect length
  - Less interconnect delay
  - Increased bandwidth
  - Reduced power
  - Heterogeneous integration

- Cross section diagram of via-mid device
- TSV formed after FEOL, before BEOL
- Current work is on 5 \( \mu \text{m} \) diameter, 50 \( \mu \text{m} \) deep vias
Common Industry Needs
- Materials and process evaluations
- Thermal Management
  - Materials, EDA
- Understanding Costs
  - Reference flows, BOM to CoO
- Technology maturity & Standards
- Supply Chain
  - Interfaces and handoffs
- Pathfinding Tools
  - Performance, power, floor planning
3D Interconnect Roadmap

First gen products underway

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Via-mid TSV Demonstration Flow

- Etch TSV, deposit liner / seed
- Fill
- TSV CMP
- M1

- TSV wafer
- Handle wafer
- Bond to handle wafer
- Grind, Stress relieve

- Cross section diagrams for the TSV-mid demonstration flow
- Steps that use CMP are highlighted
TSV Integration

Backside

- Final via reveal wet etch/CMP
- Backside dielectric
- Via planarization polish
- Backside metal

• 5 CMP steps are used to create simple via chains
• Via planarization polish and backside metal CMP present unique challenges for CMP
TSV Polish

Challenges
- Polish ~1 µm Cu overburden – High removal rate slurry
- Remaining copper and barrier
- Remove dielectric liner without dishing/smearing the Cu

• FIB / SEM section of plated TSVs
• 5 µm x 50 µm TSV
• Void-free bottom-up fill
• Less than ~1 µm overburden

Cross section diagrams show TSV formed in a via-mid process
Issues with TSV CMP

- Post TSV polish showing incoming problem with under-filled via
- Post TSV polish problem showing remaining copper
- Post TSV polish problem showing remaining barrier layer
- Successful TSV polish showing clean via
M1 CMP Issues

Post-M1 CMP problem with remaining copper

Post-M1 CMP problem with scratches

Post-M1 CMP with incoming copper puddle

Successful clean post M1 CMP surface
Wafer Bond Processes

- **Two types of bonding**
  - Permanent Bonding
  - Temporary Bonding

- **Substrate material**
  - Device wafer: 300 mm TSV patterned wafers
  - Carrier wafer: 300 mm bare Si

- **Bond material**
  - Permanent Bonding: Benzocyclobuten (BCB) adhesive
  - Temporary Bonding: Brewer Science HT 10.10/Shin Etsu TA 3000 bonding material

- **Bond Process**
  - Temporary Bonding: Carrier Wafer edge zone (high adhesion zone) width 5 mm
  - Permanent Bonding: Full Wafer Bonding

- **Bond metrology**
  - No delamination
  - No voids
  - Post bond total thickness variation (TTV) ≤ 5 µm
Backgrinding Defects (Permaneht bonding)

Post grind defect

Post grind cracks

Post grind bond material peeling and cracks

Post grind permanent bond peeling
Grind and Polish Images (Permanent Bonding)

- TEM images show no sub-surface (crystal) damage after back polish
- SEM top down images show same surface profile on Bare Si and after grinding process
Grinding Issues (Permanent Bonding)

- No explicit damage observed at bond interface due to grinding
- Bonding is still a challenge to achieve defect free thinned wafer
- Typical grind results show TTV < 5 µm & WIWNU < 5% is achievable for 50 µm target

Scanning acoustic microscope (SAM) image showing no damage to the bonded wafer

Bonded wafer with notch aligned for effective grinding

Target thickness 50 µm (Device wafer/BCB/Handle wafer)
Edge Grind Issues (Temporary Bonding)

- Images show the edge of wafers ground to 100 \( \mu \text{m} \)
- Typical chips and cracks observed after the wafer grind

- Edge Grind Thickness: 0.5 mm
- Grind Depth: 15 \( \mu \text{m} \) into the temporary bonding thickness
- TSV wafer thickness: 50 \( \mu \text{m} \) and 100 \( \mu \text{m} \)
Effect of Edge Grind on Drop Tests (Temporary Bonding)

- Cracks are observed in the thin Si wafers after drop tests
- Cracks start from edge grind chips
TSV Reveal Wet Etch

- TSV reveal etch removes Si from above and around the TSV (5-8 µm)
- Desired reveal height after the etch depends on RDL processing (1-2.5 µm)
- Reveal etch requirements:
  - Liner selectivity
  - Profile control
  - Smooth surface condition
  - Acceptable etch rate (1-3 µm/min)
- This process step is critical for TSV yield
Vias after the Reveal Wet Etch

- FIB images show the dielectric liner remains intact
- No footing is observed at the base of the via
- SEM images show the revealed TSVs and the Si surface are clean
- The silicon surface does not show pyramids or other etching defects

FIB/SEM image of revealed via

Tilt SEM images show the silicon surface is smooth, with no defects around the via
TSV Reveal – Wet vs CMP

SEM image of wet etch revealed via

Si/Cu reveal-Post bulk silicon removal (Rough surface)

Si/Cu CMP

Isolation oxide

Barrier

Post fine Si/Cu CMP for via reveal
Si/Cu CMP Challenges: Cu Residue and Dishing

Sequential polish to reveal via
Qcept Technologies has an inspection method that rapidly scans the entire wafer for work function differences.

The work function measurements are used to identify locations for secondary ion mass spectrometry (SIMS) analysis.

Cu levels are measured by SIMS at standard sites as well as additional points based on ChemetriQ inspection results.

ChemetriQ description and data courtesy of Qcept Technologies.

TOF-SIMS before vs. after clean.
Cabot / Air Products Wafer

- QCEPT workfunction scan after clean shows much cleaner wafer surface
- TOF-SIMS only shows about a 2x reduction in Cu surface concentration
TOF-SIMS Imaging

- As Polished sample showed heavy copper ion contamination virtually bridging the copper vias
- Cleaning with alkaline CP98-D was most effective in removing copper ion contamination

→ Results quantified using the standard SEMATECH analysis procedure (QCEPT scan, TOF-SIMS)

Images courtesy of Air Products
Oxide Planarization

Polish TSVs planar with the dielectric

Oxide deposited vias

Post oxide planarization vias showing Cu pillar breakage

- Oxide planarization process suffers from problems with non-uniformity in polishing and copper pillar breakage due to polish rate difference between copper and oxide
- An oxide planarization process has been developed with minimum dishing and erosion using CMC slurry
Effect of Topography on Hard and Soft pad polishing

Step 1 Polish

- Step 1, Soft pad, 180 sec polish, Sparse array
  - Center Die Dishing: 8.24 nm

- Step 1, Soft pad, 180 sec polish, Dense array
  - Center Die Dishing: 1290 nm

Effect of Soft pad Polishing (Step 1)
- Good topography on Sparse array
- Bad topography on Dense array

Step 2 Polish

- Step 2, Hard pad, 180 sec polish, Sparse array
  - Center Die Dishing: 19.38 nm

- Step 2, Hard pad, 180 sec polish, Dense array
  - Center Die Dishing: 29 nm

Effect of Hard pad Polishing (Step 2)
- Good topography on Sparse array
- Good topography on Dense array
- Candidate for single-step CMP!
Summary and Conclusions

- Grind and CMP processes are critically important steps in TSV processing
- Areas for development include
  - Via-mid TSV polish
  - Via planarization polish
  - Via expose polish
  - Planar and reveal processes